## IN THE CLAIMS

This listing of claims will replace all prior versions and listing of claims in the application:

1. (withdrawn) An interconnect assembly comprising:

a base layer;

an interconnection circuit fabricated on said base layer comprising one or more layers of conductive traces with intervening dielectric material, said interconnection circuit having exposed input/output pads on a top layer, wherein said input/output pads are connected to selected ones of said conductive traces in said interconnection circuit;

an additional layer of dielectric material fabricated on top of said interconnection circuit that is patterned to create wells at each of said input/output pads; and

conductive material filling said wells.

2. (withdrawn) The interconnect assembly of Claim 1 wherein said base layer is flexible.

3. (withdrawn) The interconnect assembly of Claim 1 wherein said base layer is rigid.

4. (withdrawn) The interconnect assembly of Claim 3 wherein said rigid base layer is a glass substrate.

5. (withdrawn) The interconnect assembly of Claim 1 wherein said base layer is a silicon wafer.

6. (withdrawn) The interconnect assembly of Claim 1 wherein said conductive traces have a minimum pitch of 20 microns or less.

7. (withdrawn) The interconnect assembly of Claim 1 wherein said wells are spaced apart with a minimum pitch of less than 200 microns.

8. (withdrawn) The interconnect assembly of Claim 1 wherein said conductive material filling said wells includes solder.

9. (withdrawn) The interconnect assembly of Claim 1 wherein said conductive material filling said wells is an indium-based solder such as Indalloy 290 containing 97% In and 3% Ag.

10. (withdrawn) An electronic assembly comprising:

a base layer;

one or more electronic components having a conductive bump at each input/output pad of each of said components;

an interconnection circuit fabricated on said base layer comprising one or more layers of conductive traces with intervening dielectric material, said interconnection circuit having at least one exposed input/output pad on a top layer for each of said bumps, wherein said input/output pads are connected to selected ones of said conductive traces in said interconnection circuit;

surface depressions forming wells at each of said input/output pads; and

conductive material filling said wells;

wherein said bumps are mated with said conductive material filling said wells to mechanically attach and electrically connect said electronic components to said interconnection circuit at said input/output pads of said interconnection circuit.

11. (withdrawn) An electronic assembly comprising:

a base layer;

one or more electronic components having a conductive bump at each input/output pad of each of said components;

an interconnection circuit fabricated on said base layer comprising one or more layers of conductive traces with intervening dielectric material, said interconnection circuit having exposed input/output pads on a top layer, wherein said input/output pads are connected to selected ones of said conductive traces in said interconnection circuit;

an additional layer of dielectric material fabricated on top of said interconnection circuit that is patterned to create wells at each of said input/output pads; and

conductive material filling said wells;

wherein said bumps are mated with said conductive material filling said wells to mechanically attach and electrically connect said electronic components to said interconnection circuit at said input/output pads of said interconnection circuit.

12. (withdrawn) An electronic assembly comprising:

a base layer;

one or more electronic components having a conductive bump at each input/output pad of each of said components;

one or more access cables having a conductive bump at each input/output pad of each of said access cables;

an interconnection circuit fabricated on said base layer comprising one or more layers of conductive traces with intervening dielectric material, said interconnection circuit having exposed input/output pads on a top layer, wherein said input/output pads are connected to selected ones of said conductive traces in said interconnection circuit;

an additional layer of dielectric material fabricated on top of said interconnection circuit that is patterned to create wells at each of said input/output pads; and

conductive material filling said wells;

wherein said bumps of said components and said bumps of said access cables are mated with said conductive material filling said wells to mechanically attach and electrically connect said components and said access cables to said interconnection circuit at said input/output pads of said interconnection circuit.

13. (withdrawn) The electronic assembly of Claims 10-12 wherein said electronic components are integrated circuit chips in bare die form.

14. (withdrawn) The electronic assembly of Claims 10-12 wherein said conductive bumps are stud bumps.

15. (withdrawn) The electronic assembly of Claim 10-12 wherein said electronic components are thermally coupled to a heat sink.

16. (withdrawn) The electronic assembly of Claim 15 wherein said thermal coupling includes a thin layer of thermally conductive material between faces of said components or films covering said faces and a surface of said heat sink.

17. (withdrawn) An electronic assembly comprising:

an interconnection circuit having wells filled with conductive material at some or all of its input/output pads; and,

one or more module access cables having a conductive bump at some or all of its input/output pads;

wherein said conductive bumps are mated with said wells of said interconnection circuit in a one to one relationship.

18. (withdrawn) An electronic assembly comprising:

an interconnection circuit having wells filled with conductive material at some or all of its input/output pads;

one or more components having a conductive bump at some or all of its input/output pads; and

one or more module access cables having a conductive bump at some or all of its input/output pads;

wherein said conductive bumps of said components and said module access cables are mated with said wells of said interconnection circuit in a one to one relationship.

19. (original) A method for fabricating an electronic circuit comprising the steps of:

providing a rigid carrier;

applying a base dielectric layer on said rigid carrier;

fabricating one or more interconnection circuits having exposed input/output pads on said base layer;

fabricating wells at said input/output pads of said interconnection circuits; and

filling said wells with conductive material.

20. (original) The method of Claim 19 and including the additional step of attaching electronic components to said interconnection circuits to form an electronic assembly, wherein each of said components has a conductive bump at each of its input/output pads, and each of said conductive bumps is inserted into said conductive material in one of said wells.

21. (original) The method of Claims 19 and 20 and including the step of fabricating a release layer interposed between said rigid carrier and said base dielectric layer.

22. (original) The method of Claim 21 and including the step of separating said interconnection circuit or electronic assembly from said rigid carrier at said release layer, after completing said circuit or assembly.

23. (original) The method of Claims 19-22 wherein said interconnection circuits comprise multiple dielectric and conducting layers.

24. (original) The method of Claim 23 wherein said dielectric layers are polymer layers that are patterned using light projected through a mask.

25. (original) The method of Claim 24 wherein said release layer is a fluorinated silicone.

26. (original) The method of Claim 21 wherein said release layer is not present near the edges of said rigid carrier, to provide an edge region of strong adhesion between said base dielectric layer and said rigid carrier.

27. (original) The method of Claim 26 wherein said release layer is additionally not present in streets at the periphery of a plurality of said interconnection circuits.

28. (original) The method of Claim 19 wherein said wells are filled with said conductive material using a squeegee.

29. (original) The method of Claim 19 wherein said wells are formed with essentially vertical walls.

30. (withdrawn) An electronic cable having built-in connection means comprising:

a base layer;

an interconnection circuit fabricated on said base layer, said interconnection circuit including conductive traces;

wherein said traces terminate at bonding pads of said cable, and said bonding pads are arrayed to form cable ports with at least one input port and at least one output port per cable;

wherein each of said ports includes a connection means at each of said bonding pads; and,

wherein said connection means is implemented using either conductive bumps or wells filled with conductive material.

31. (withdrawn) The electronic cable of Claim 30 wherein said cable is formed into multiple fingers and each of said fingers includes one or more of said ports.

32. (withdrawn) The electronic cable of Claim 30 wherein one or more of said ports has a redistributed array of said bonding pads, with increased spacing between said pads.

33. (withdrawn) A stacked contact formed between a plurality of conductive layers of an interconnection circuit comprising:

planarizing layers of dielectric material between each of said conductive layers; and

contact windows having tapered walls in each of said planarizing layers, said contact

windows positioned above connection points on preceding metal layers and below connection points on succeeding metal layers.

34. (withdrawn) The stacked contact of Claim 33 wherein said contact windows are photo-defined.

35. (withdrawn) The stacked contact of Claim 33 wherein trace stubs are provided at each conducting layer of the stacked contact.

36. (withdrawn) A multi-layer interconnection circuit wherein stacked contacts with trace stubs are provided at input/output pads of said interconnection circuit.

37. (original) A trace routing method for a multi-layer interconnection circuit comprising the steps of:

providing stacked contacts with trace stubs at input/output pads of said interconnection circuit; and

limiting contacts between conductive layers to two-level contacts in routing areas where maximum routing density is desired.

38. (original) A method for forming wells filled with conductive material on an interconnect circuit comprising the steps of:

applying a layer of dielectric material on top of said interconnect circuit;

forming openings in said dielectric layer at each input/output pad of said interconnect circuit; and

depositing said conductive material in said openings to form wells filled with conductive material.

39. (original) The method of Claim 38 wherein said conductive material is deposited in said openings using a squeegee.

40. (original) A method for assembling an integrated circuit chip having input/output pads on an interconnection circuit having bonding sites corresponding to said input/output pads comprising the steps of:

providing a conductive bump at each of said input/output pads;

fabricating wells filled with solder at each of said bonding sites;

inserting said conductive bumps into said wells filled with solder; and

heating and cooling said solder to make permanent connections.

41. (original) The method of Claim 40 wherein said interconnection circuit is flexible.

42. (withdrawn) A circuit assembly comprising:

a plurality of integrated circuits having conductive bumps at each input/output pad;

an interconnection circuit having wells filled with solder, said wells corresponding in a one-to-one relationship with said conductive bumps of said integrated circuits; and

bonding at each of said pads said conductive bumps to said solder in each of said wells to form a permanent connection.

43. (withdrawn) The circuit assembly of Claim 42 wherein said interconnection circuit is flexible.

44. (original) A method for reworking defective components mounted on a circuit substrate wherein a conductive bump is provided at each bonding site of each of said components and a corresponding well filled with solder is provided at each bonding site on said circuit substrate, comprising the steps of:

heating said circuit substrate and selectively heating said defective component until said solder at each of said wells of said defective circuit melts;

withdrawing said defective component from said wells;

cleaning the area surrounding said wells as required;

adding solder to said wells as required;

inserting the conductive bumps of a replacement component in said wells;

heating said circuit substrate and said replacement component until said solder melts and said conductive bumps are fully inserted in said wells; and

cooling until said melted solder solidifies to form a permanent bond.

45. (original) The method of Claim 44 wherein said conductive bumps are stud bumps.

46. (withdrawn) A circuit assembly that may be reworked to replace a defective component, comprising:

a base layer;

an interconnection circuit having input/output pads fabricated on said base layer;

wells filled with solder fabricated on said interconnection circuit at said input/output pads;

components having conductive bumps at connection points; and

wherein said conductive bumps are mated with said wells filled with solder to form re-workable bonds.

47. (withdrawn) A module access port for an electronic module comprising:

a set of module access pads;

a well formed from dielectric material at each of said module access pads; and

conductive material filling each of said wells.

48. (withdrawn) A hermetically sealed electronic circuit module having attached components comprising:

a module access port including an array of module access pads;

a dielectric layer coating said circuit module at surfaces having attached components, with openings at said module access pads; and

a continuous metal film coating the entire surface of said circuit module, except for said openings at said module access pads.

49. (withdrawn) An electro-magnetically shielded electronic circuit module having attached components comprising:

a module access port including an array of module access pads;

a dielectric layer coating said circuit module at surfaces having attached components with openings at said module access pads; and

a continuous metal film coating the entire surface of said circuit module, except for said openings at said module access pads.

50. (withdrawn) The electro-magnetically shielded circuit module of Claim 49 wherein said continuous metal film is grounded.